IN THE CLAIMS

1. (currently amended) A clock signal duty cycle stabilization circuit, comprising:

an edge detection circuit configured to receive an external clock signal and generate an output therefrom;

a conditioning circuit for producing a conditioned signal having a one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

a latch circuit coupled to receive the output from the edge detection circuit, the latch circuit configured to produce a rising edge of an internal clock signal and a falling edge of the internal clock signal in accordance with the output of the edge detection circuit, wherein the rising edge of the internal clock signal is triggered at a rising edge of the external clock signal by the edge detection circuit.

2. (original) The clock signal duty cycle stabilization circuit of claim 1, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

3. (original) The clock signal duty cycle stabilization circuit of claim 1, wherein the latch circuit comprises an R-S latch, the R-S latch configured to

receive the output of the edge detection circuit and generate the rising edge and the falling edge therefrom.

4. (cancelled)

5. (original) The clock signal duty cycle stabilization circuit of claim 1, wherein the external clock signal is a reference clock signal from an external source.

6. (original) The clock signal duty cycle stabilization circuit of claim 1, wherein the internal clock signal is a 50% duty cycle clock signal for use by an analog to digital converter.

7. (currently amended) An analog to digital converter system, comprising:

an analog to digital converter circuit for converting analog signals into digital signals;

a clock signal duty cycle stabilization circuit coupled to the analog to digital converter circuit, the clock signal duty cycle stabilization circuit configured to produce an internal clock signal for use by the analog to digital converter circuit, the clock signal duty cycle stabilization circuit further comprising:

an edge detection circuit configured to receive the external clock signal and generate an output therefrom;

a conditioning circuit for producing a conditioned signal having a one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

a latch circuit coupled to receive the output from the edge detection circuit, the latch circuit configured to produce a rising edge of the internal clock signal and a falling edge of the internal clock signal in accordance with the output of the edge detection circuit, wherein the rising edge of the internal clock signal is triggered at a rising edge of the external clock signal by the edge detection circuit.

8. (original) The system of claim 7, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

9. (original) The system of claim 7, wherein the latch circuit comprises an R-S latch, the R-S latch configured to receive the output of the edge detection circuit and generate the rising edge and the falling edge therefrom.

10. (cancelled)

11. (original) The system of claim 7, wherein the external clock signal is a reference clock signal from an external source.

12. (original) The system of claim 7, wherein the internal clock signal is a 50% internal clock signal for use by an analog to digital converter.

13. (currently amended) A clock signal duty cycle stabilization circuit, comprising:

an edge detection circuit configured to receive an external clock signal and generate an output therefrom;

a VCRO circuit for producing a VCRO signal having a one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

a timing generator circuit coupled to receive the output from the edge detection circuit, the timing generator circuit configured to produce an internal clock signal in accordance with a setting and resetting of the timing generator circuit by the output of the edge detection circuit, wherein the rising edge of the external clock signal sets the timing generator circuit to produce a rising edge of the internal clock signal and the VCRO signal resets the timing generator circuit to produce a falling edge of the internal clock signal.

14. (original) The clock signal duty cycle stabilization circuit of claim 13, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

15. (original) The clock signal duty cycle stabilization circuit of claim 13, wherein the timing generator circuit comprises a non overlapping clock generator, the non overlapping clock generator configured to receive the output of the edge detection circuit and generate a rising edge of the internal clock signal therefrom.

16. (cancelled)

17. (original) The clock signal duty cycle stabilization circuit of claim 13, wherein the external clock signal is a reference clock signal from an external source.

18. (original) The clock signal duty cycle stabilization circuit of claim 13, wherein the internal clock signal is for use by an analog to digital converter coupled to the clock signal duty cycle stabilization circuit.

19. (currently amended) An analog to digital converter system, comprising:

an analog to digital converter circuit for converting analog signals into digital signals;

a clock signal duty cycle stabilization circuit coupled to the analog to digital converter circuit, the clock signal duty cycle stabilization circuit configured to produce an internal clock signal for use by the analog to digital converter circuit, the clock signal duty cycle stabilization circuit further comprising:

an edge detection circuit configured to receive an external clock signal and generate an output therefrom;

a VCRO circuit for producing a VCRO signal having a one half clock period delayed phase with respect to the external clock signal and for use by the edge detection circuit; and

a timing generator circuit coupled to receive the output from the edge detection circuit, the timing generator circuit configured to produce an internal clock signal in accordance with a setting and resetting of the timing generator circuit by the output of the edge detection circuit, wherein the rising edge of the external clock signal sets the timing generator circuit to produce a rising edge of the internal clock signal and the VCRO signal resets the timing generator circuit to produce a falling edge of the internal clock signal.

20. (original) The system of claim 19, wherein the edge detection circuit comprises a NAND gate coupled to a delay element, the NAND gate

having an input to receive the external clock signal and an output for producing the output of the edge detection circuit.

21. (original) The system of claim 19, wherein the timing generator circuit comprises a non overlapping clock generator, the non overlapping clock generator configured to receive the output of the edge detection circuit and generate a rising edge of the internal clock signal therefrom.

22. (cancelled)

23. (original) The system of claim 19, wherein the external clock signal is a reference clock signal from an external source.

24. (cancelled)